IN THE CLAIMS

Claims 1-22 (Cancelled)

23. (Currently amended) A processing device, comprising:

a reconfigurable circuit formed of a logic circuit, allowing change in function;

an internal state holding circuit receiving an output of said reconfigurable circuit;

a first path portion transmitting the ~~an~~ output of said reconfigurable circuit received by said internal state holding circuit as an input to said reconfigurable circuit;

a setting portion supplying setting data for configuring an intended circuit in said reconfigurable circuit; and

a control portion controlling said setting portion such that a plurality of setting data are successively supplied to said reconfigurable circuit, so that an output of [[a]] an intended circuit configured on said reconfigurable circuit in accordance with one setting data is supplied to an input of [[a]] an intended circuit configured in accordance with setting data next to said one ~~next~~ setting data through said first path portion; ~~and~~

~~an internal state holding circuit receiving an output of said reconfigurable circuit,~~

~~said internal state holding circuit being connected to said first path portion;~~

~~said device further comprising:~~

a memory portion operating at a lower speed than said internal state holding circuit, storing ~~in a prescribed area~~ an output of [[a]] an intended circuit configured on said reconfigurable circuit in a prescribed area in accordance with ~~said~~ one setting data; and

a second path portion transmitting an ~~the~~ output of the circuit configured on said reconfigurable circuit stored in said prescribed area of said memory portion as an input to a circuit configured in accordance with the ~~next~~ setting data subsequent to said one setting data.

Claim 24 (Cancelled)

25. (Previously presented) The processing device according to claim 23, wherein

said setting portion successively supplies a plurality of setting data to said reconfigurable circuit, so that one circuit is formed as a whole.

26. (Previously presented) The processing device according to claim 23, wherein

said plurality of setting data represent a plurality of divided circuits obtained by dividing one circuit.

27. (Previously presented) The processing device according to claim 23, wherein

said reconfigurable circuit is configured as a combinational circuit.

28. (Previously presented) The processing device according to claim 23, further comprising:

an output circuit receiving an output of said reconfigurable circuit,

said output circuit providing the output of said reconfigurable circuit when said reconfigurable circuit is configured a plurality of times by said setting portion.

29. (Previously presented) The processing circuit according to claim 23, further comprising:

a switching circuit switching between the input from said second path portion and an external input, to be an input to said reconfigurable circuit.

30. (Previously presented) The processing device according to claim 23, wherein

said reconfigurable circuit includes a plurality of logic circuits each capable of selectively executing a plurality of operation functions, and a connecting portion allowing setting of a connection relation among the logic circuits; and

said setting portion sets the functions and said connection relation of said logic circuits.

31. (Previously presented) The processing device according to claim 30, wherein

said logic circuit is an arithmetic logic circuit capable of selectively executing a plurality of multi-bit operations.

Claims 32 and 33 (Cancelled)

34. (Currently amended) A processing device, comprising:

a reconfigurable circuit allowing change in function and connection relation;

a setting portion storing setting data representing a divided unit forming a part of an intended circuit, and supplying the setting data to said reconfigurable circuit; and

a control portion controlling said setting portion such that a plurality of setting data are successively supplied according to a process flow to said reconfigurable circuit to configure said intended circuit; wherein

said reconfigurable circuit has at least one state holding circuit holding an internal state;

said reconfigurable circuit is divided, by an arrangement of said state holding circuit, into a plurality of stages of reconfigurable units; and

said control portion controls

at one time point,

said setting portion such that setting data of a divided unit configuring an intended circuit is supplied to a reconfigurable unit at a predetermined stage,

at a next time point,

said setting porting such that setting data of a next divided unit configuring said intended circuit is supplied to said reconfigurable unit at a stage next to said predetermined stage,

said setting portion such that setting data of a divided unit configuring a circuit different from said intended circuit is supplied to said reconfigurable unit of said predetermined stage;

said reconfigurable circuit including a path portion to input an output of the reconfigurable unit of the last stage to the reconfigurable unit of the first stage.

~~said setting portion such that when a plurality of intended circuits are to be configured, setting data for configuring divided units each forming a part of the circuits on respective ones of said plurality of stages of reconfigurable units are successively supplied along a process flow.~~

Claims 35-36 (Cancelled)

37. (Previously presented) The processing device according to claim 34, wherein a reconfigurable unit is configured as a combinational circuit.

38. (Previously presented) The processing device according to claim 34, further comprising:

an output circuit receiving an output of said reconfigurable circuit,

said output circuit providing the output of said reconfigurable circuit when said reconfigurable circuit is configured a plurality of times by said setting portion.

39. (Previously presented) The processing circuit according to claim 34, further comprising:

an internal state holding circuit receiving an output of said reconfigurable circuit; and

a first path portion inputting the output signal held by said internal state holding circuit to the first stage of reconfigurable units.

40. (Previously presented) The processing device according to claim 39, further comprising:

a memory portion storing in a prescribed area an output of said reconfigurable circuit in accordance with a setting data; and

a second path portion transmitting the output of the circuit configured on said reconfigurable circuit stored in said prescribed area of said memory portion as an input to a circuit configured in accordance with the next setting data.

41. (Previously presented) The processing circuit according to claim 40, further comprising:

a switching circuit switching between the input from said second path portion and an external input, to be an input to said reconfigurable circuit.

42. (Previously presented) The processing device according to claim 34, wherein

a reconfigurable unit includes a plurality of logic circuits each capable of selectively executing a plurality of operation functions, and a connecting portion allowing setting of connection relation among the logic circuits; and

said setting portion sets the functions and said connection relation of said logic circuits.

43. (Previously presented) The processing device according to claim 42, wherein

said logic circuit is an arithmetic logic circuit capable of selectively executing a plurality of multi-bit operations.